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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/450,912	11/29/1999	BRIAN JOSEPH McNAMARA	17481	8320

7590                    07/14/2004

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[REDACTED] EXAMINER

SMITH, SHEILA B

ART UNIT	PAPER NUMBER
2681	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/450,912	MCNAMARA, BRIAN JOSEPH
	<b>Examiner</b>	<b>Art Unit</b>
	Sheila B. Smith	2681

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 29 April 2004.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 9-15 and 19-21 is/are allowed.
- 6) Claim(s) 1-7 and 16-18 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                     | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-7, are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh (U. S. Patent Number 5,995,814).

*Regarding claim 1*, Yeh discloses essentially all the claimed invention as set forth in the instant application, further Yeh discloses single stage dual-band low-noise amplifier for use in a wireless communication system receiver. In addition Yeh discloses a first impedance element (L1) and a second impedance element (L2) between an RF input port (IN) and an RF output port (OUT) (as exhibited in figure 1), the tuning circuit being tuned by the first and second impedance elements (L1, L2) to receive a first RF signal and to provide the first RF signal at the output port, the tuning circuit being tuned by the first impedance element alone (which reads on subset) to receive a second RF signal and to provide the second RF signal at the output port (which reads on column 10 lines 21-25), a switching transistor (Q1) being switched on and off by changing its bias voltage, a band control voltage source (V1, V2) connected to the switching transistor to change its bias voltage, and the switching transistor (Q1) having conducting gates (emitter) connected to the second impedance element (L2) to short the second impedance

element, which tunes the tuning circuit by the first impedance element (L1) (which reads on column 4 lines 32-35).

***Regarding claim 2,*** Yeh discloses a first and second impedance elements are inductance impedance elements (L1, L2).

***Regarding claims 3 and 7,*** Yeh discloses a first and second impedance elements are capacitance impedance elements (C1, C3).

***Regarding claim 4,*** Yeh discloses a conducting drain and source nodes of the switching transistor (Q1) being in parallel connection with the second impedance element (L2) to open circuit the second impedance element.

***Regarding claim 5,*** Yeh discloses a first and second impedance elements are inductance impedance elements (L1, L2).

***Regarding claim 6,*** Yeh discloses a resistance (R1) connected across the conducting gates of the switching transistor (Q1), the source of band control voltage (V1, V2) being connected to a dividing point of the resistance, and the conducting drain and source nodes of the switching transistor (Q1) being in series connection with the second impedance element (L2) to open-circuit the second impedance element (as exhibited in figure 5).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh.

***Regarding claim 16,*** Yeh discloses the circuit of claim 1 as described above. Yeh, however, fails to disclose the use of a MESFET transistor.

Official notice is taken that the use of a MESFET transistor for a switching transistor is well known in the art. Therefore, it would have been obvious to a person of ordinary skill in the art to use any well known transistor, including the well known MESFET transistor to implement the required switching circuitry in Yeh for the purpose of providing low distortion power application.

***Regarding claims 17 and 18,*** Yeh discloses a switching transistor (Q1) is integrally formed with the tuning circuit in a single integrated circuit (which reads on column 4 lines 32-35).

***Allowable Subject Matter***

3. ***Claim 8*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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4. ***Claims 9-15,19-21 allowed.***

***Claim 9*** is allowed. The following is an examiner's statement of reasons for allowance: The prior art of record considered alone or in combination neither anticipates nor renders a dual band RF circuit with a first impedance element and a second impedance element between an RF input port and an RF output port, the tuning circuit being tuned by the first and second impedance elements to receive a first RF signal and to provide the first RF signal at the output port, the tuning circuit being tuned by the first impedance element alone to receive a second RF signal and to provide the second RF signal at the output port, a switching transistor being switched on and off by changing its bias voltage, the second switching transistor having conducting drain and source nodes connected to the second the second capacitance impedance element, which tunes the tuning circuit by the first capacitance impedance element.

The prior art of record provided numerous teachings of a dual band RF circuit with a first impedance element and a second impedance element between an RF input port and an RF output port. However, the prior art of record failed to specifically disclose the second switching transistor having conducting drain and source nodes connected to the second the second capacitance impedance element, which tunes the tuning circuit by the first capacitance impedance element.

5. Regarding claims 10-15,19-21, are allowed as being dependent upon independent base claims that have been allowed.

***Response to Arguments***

6. Applicant's arguments filed 4/29/04 have been fully considered but they are not persuasive.

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Regarding applicants arguments concerning there being no switching transistor disclosed in Yeh, the examiner disagrees Yeh, discloses at column 4 lines 32-37, "the capacitor C3 serves as a bypass capacitor, to shunt the emitter of Q1 to ground potential at RF frequencies such that the emitter biasing resistor R1 will not degrade the high-frequency transistor gain", the examiner contends that this section reads on switching because shunting the emitter the signal takes a different path which reads on switching.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheila B. Smith whose telephone number is (703)305-0104. The examiner can normally be reached on Monday-Thursday 6:00 am - 3:00 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Erika Gary can be reached on 703-308-0123. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Smith   
July 11, 2004

  
SINH TRAN  
PRIMARY EXAMINER